CMLDM7003E
CMLDM7003JE
ENHANCED SPECIFICATION

SURFACE MOUNT PICOmini™
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET

ENHANCED SPECIFICATION

PICOmini™

SOT-563 CASE

Central™
Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM7003E and CMLDM7003JE are Enhancement-mode N-Channel Field Effect Transistors, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7003E utilizes the USA pinout configuration, while the CMLDM7003JE utilizes the Japanese pinout configuration. These special Dual Transistor devices offer low drain-source on state resistance ($r_{DS(ON)}$) and ESD protection up to 2kV.

MARKING CODE: CMLDM7003E: C73
CMLDM7003JE: C7J

FEATURES

- **ESD protected up to 2kV**

ENHANCED SPECIFICATIONS

I_{GSSF}, I_{GSSR}, V_{GS}=5V	50nA Max from 100nA Max
I_{GSSF}, I_{GSSR}, V_{GS}=10V	0.5μA Max from 2.0μA Max
I_{GSSF}, I_{GSSR}, V_{GS}=12V	1.0μA Max from 2.0μA Max
$r_{DS(ON)}$, V_{GS}=1.8V, I_D=50mA	2.3Ω Max from 3.0Ω Max
$r_{DS(ON)}$, V_{GS}=2.5V, I_D=50mA	1.9Ω Max from 2.5Ω Max
$r_{DS(ON)}$, V_{GS}=5.0V, I_D=50mA	1.5Ω Max from 2.0Ω Max

MAXIMUM RATINGS (T_A=25°C)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage	V_{DG}	50	V
Gate-Source Voltage	V_{GS}	12	V
Continuous Drain Current	I_D	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Power Dissipation	P_D	350	mW (Note 1)
Power Dissipation	P_D	300	mW (Note 2)
Power Dissipation	P_D	150	mW (Note 3)
Operating and Storage Junction Temperature	T_J,T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JA}	357	°C/W

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm^2
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm^2
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm^2

R1 (18-December 2006)

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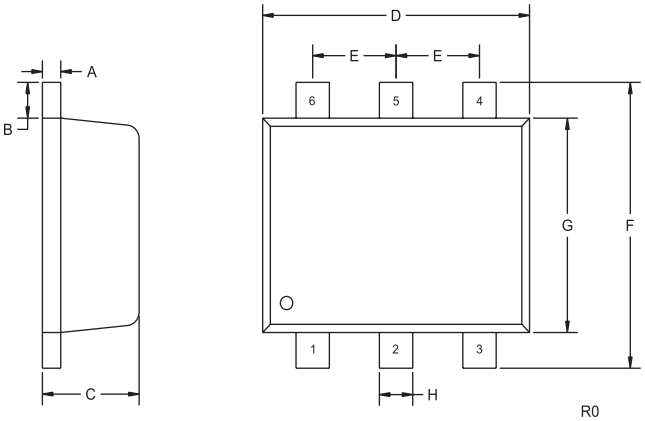
ELECTRICAL CHARACTERISTICS PER TRANSISTOR (T_A=25°C unless otherwise noted)

	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
♦	**I_{GSSF}, I_{GSSR}**	**V_{GS}=5V**			**50**	nA
♦	**I_{GSSF}, I_{GSSR}**	**V_{GS}=10V**			**0.5**	µA
♦	**I_{GSSF}, I_{GSSR}**	**V_{GS}=12V**			**1.0**	µA
	I_{DSS}	V_{DS}=50V, V_{GS}=0V			50	nA
	BV_{DSS}	V_{GS}=0V, I_D=10µA	50			V
	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250µA	0.49		1.2	V
♦	**$r_{DS(ON)}$**	**V_{GS}=1.8V, I_D=50mA**		**1.6**	**2.3**	Ω
♦	**$r_{DS(ON)}$**	**V_{GS}=2.5V, I_D=50mA**		**1.3**	**1.9**	Ω
♦	**$r_{DS(ON)}$**	**V_{GS}=5.0V, I_D=50mA**		**1.1**	**1.5**	Ω
	g_{FS}	V_{DS}=10V, I_D=200mA	200			mmhos
	C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			5.0	pF
	C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			50	pF
	C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			25	pF
	V_{SD}	V_{GS}=0V, I_S=115mA			1.4	V

♦ ENHANCED SPECIFICATION

SOT-563 CASE - MECHANICAL OUTLINE

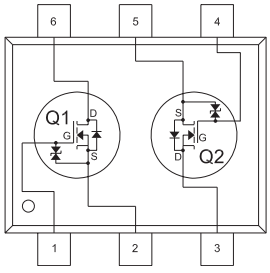


R0

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.004	0.007	0.10	0.18
B	0.008		0.20	
C	0.022	0.024	0.56	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.061	0.067	1.55	1.70
G	0.047		1.20	
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R0)

CMLDM7003E (USA Pinout)



LEAD CODE:
1) GATE Q1
2) SOURCE Q1
3) DRAIN Q2
4) GATE Q2
5) SOURCE Q2
6) DRAIN Q1

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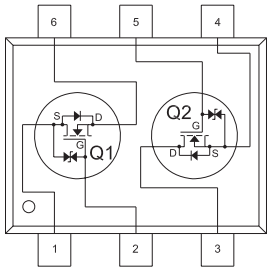
CMLDM7003JE (Japanese Pinout)



LEAD CODE:
1) SOURCE Q1
2) GATE Q1
3) DRAIN Q2
4) SOURCE Q2
5) GATE Q2
6) DRAIN Q1

MARKING CODE: C7J

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